



**Simulation Interoperability
Standards Organization**

“Simulation Interoperability & Reuse through Standards”

Workshop theme for Fall 2018: “Leveraging the Power of Simulation”

Performance of Dead Reckoning Algorithms Across Technology Eras

18F-SIW-011

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David Ronnfeldt, Australian Defence Simulation & Training Centre, Australia***



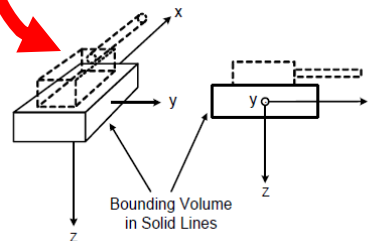
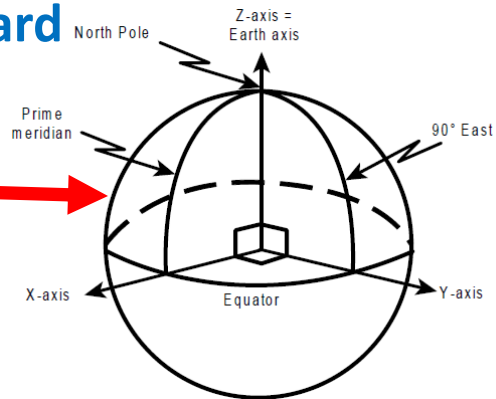
Outline of Presentation

- **Dead Reckoning in Distributed Interactive Simulation**
- **1994 Towers and Hines paper**
- **Method of determining performance**
- **Results from 1994, modern desktop systems, single board systems**
- **Comparison of performance 1994 → Present**
- **Implications for future versions of DIS**



Dead Reckoning in Distributed Interactive Simulation

- Dead reckoning used to limit rate at which simulated entities need to update position, velocity, orientation etc
- Standard set of 9 algorithms provided in IEEE standard
 - 1 – static entities
 - 2 – 5 world-referenced coordinates
 - 6 – 9 body-referenced coordinates
- Other DRAs can be developed as required





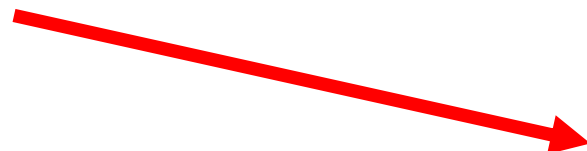
Towers and Hines 1994 Paper

- Towers, J. and Hines, J. (1994). *Highly Dynamic Vehicles in a Real/Simulated Virtual Environment: Equations of Motion of the DIS 2.0.3 Dead Reckoning Algorithms*. Report 94-57, Defense Advanced Research Projects Agency
- Commissioned by DARPA to examine dead reckoning
- Equations of motion for dead reckoning defined (referenced in latest DIS IEEE 2012)
- Two test cases run: DRA 4 and DRA 8 with different initial conditions
- Performance measured for four 1994 era systems
- Benchmark results and C code provided!



Floating Point Operations for DRAs

- DRA time determined by number of FLOPS in algorithm
- Multiplication /Division slower than Addition/Subtraction
- Trig functions (cos/sine) slower still
- No of FLOPS only provides qualitative measure of performance due to different processor architectures



Algorithm	Model	No of Floating Point Operations
1	Static	15
2	FPW	47
3	RPW	110
4	RVW	99
5	FVW	43
6	FPB	50
7	RPB	125
8	RVB	177
9	FVB	115

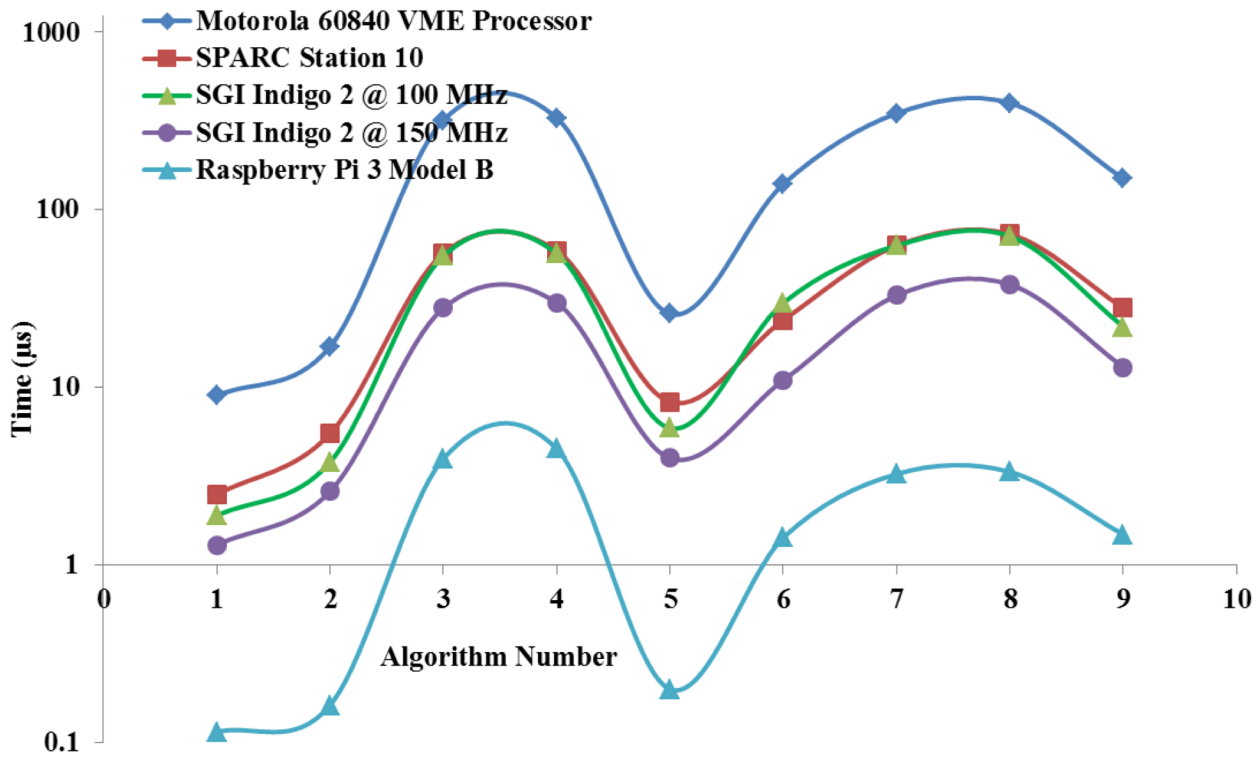


Measuring Dead Reckoning Performance

1. C function *clock_gettime()* used to determine elapsed time
2. Create an array of 1000 identical PDUs for first test case
3. Measure the elapsed time to perform dead reckoning for array of PDUs for the first test case using initial values from Towers and Hines
4. Repeat the process for the second test case
5. Average processor time over 1000 PDUs and both test cases to get mean value of processing time
6. Metric for system $i = \sum_{j=1}^{j=9} T_j^1 / \sum_{j=1}^{j=9} T_j^i$



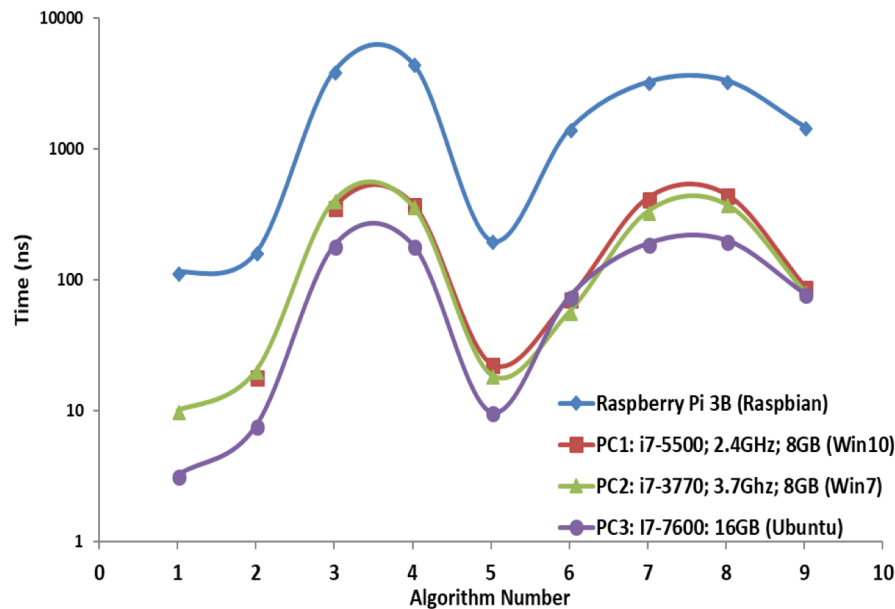
1994 Results





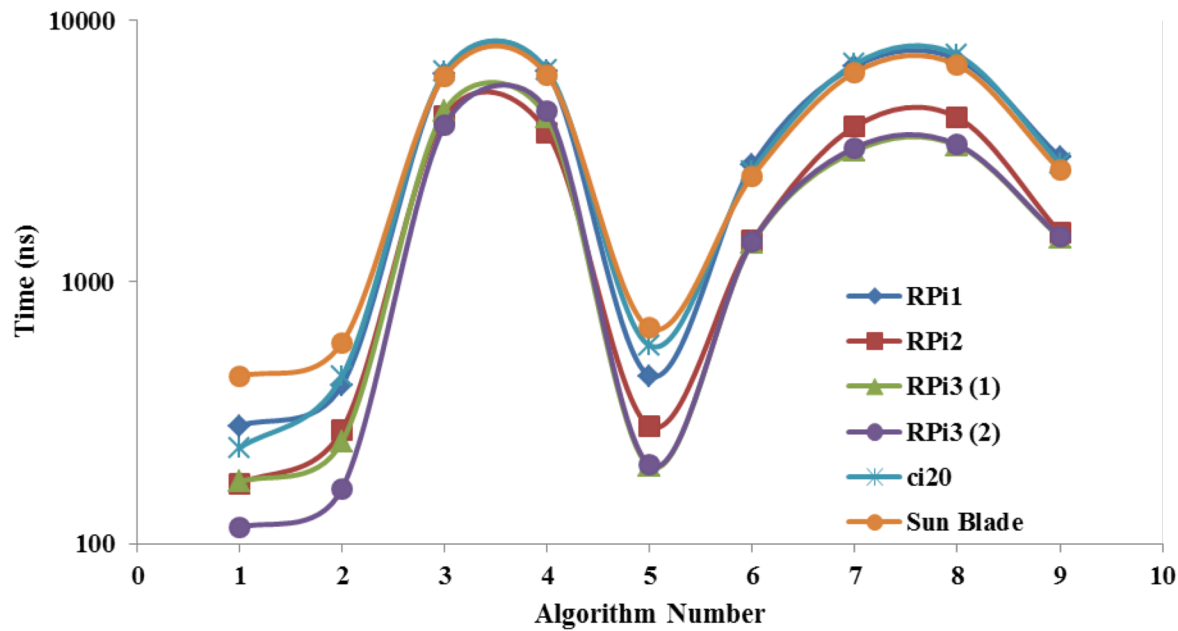
Modern Systems Tested

- Raspberry Pi models 1, 2, 3
- Desktop Intel PC
- Notebook Intel PC
- Performance Intel PC
- Creator Ci20
- Sun Blade
- G4 Power Mac
- Linux or Cygwin for Windows Systems



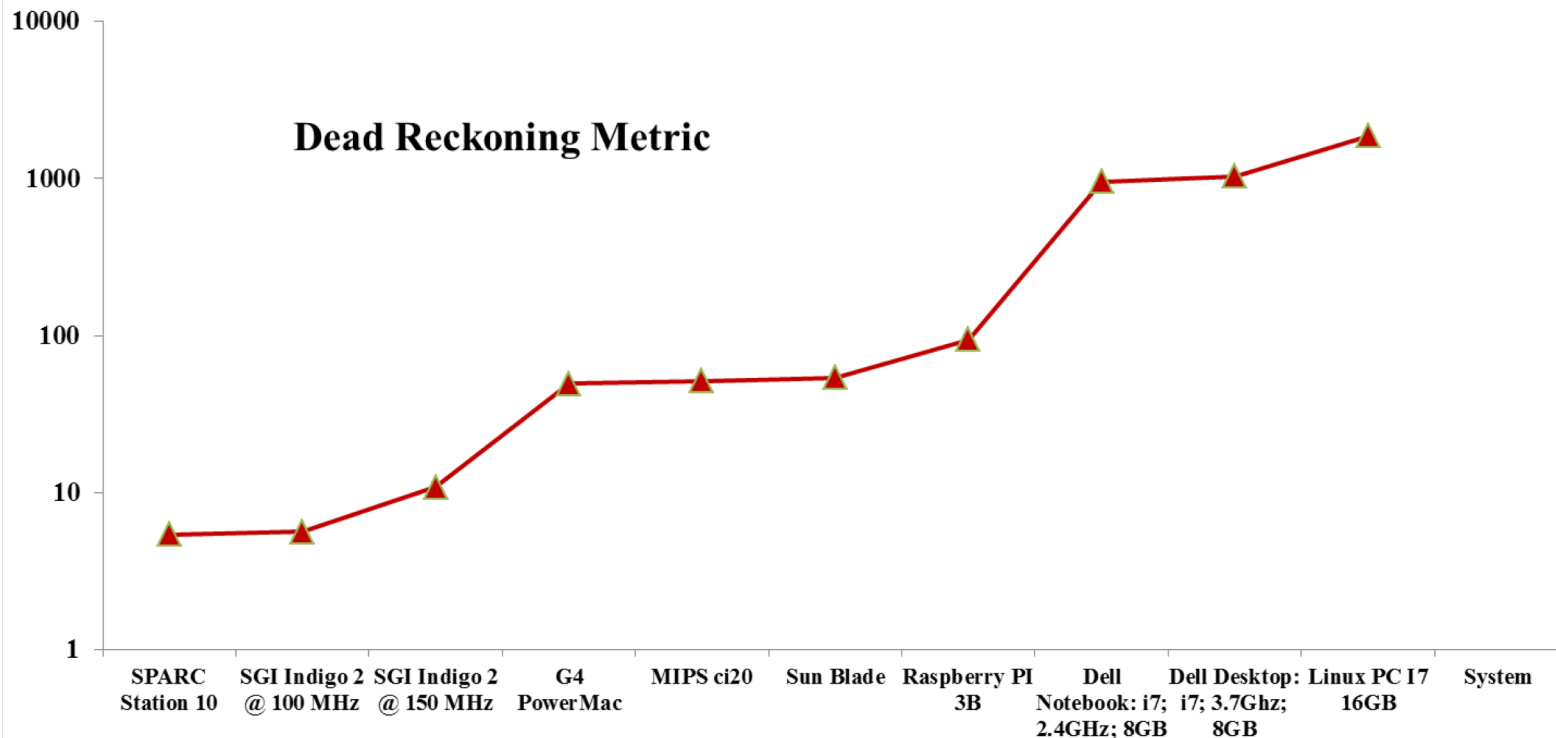


Single Board Systems





Dead Reckoning Metric

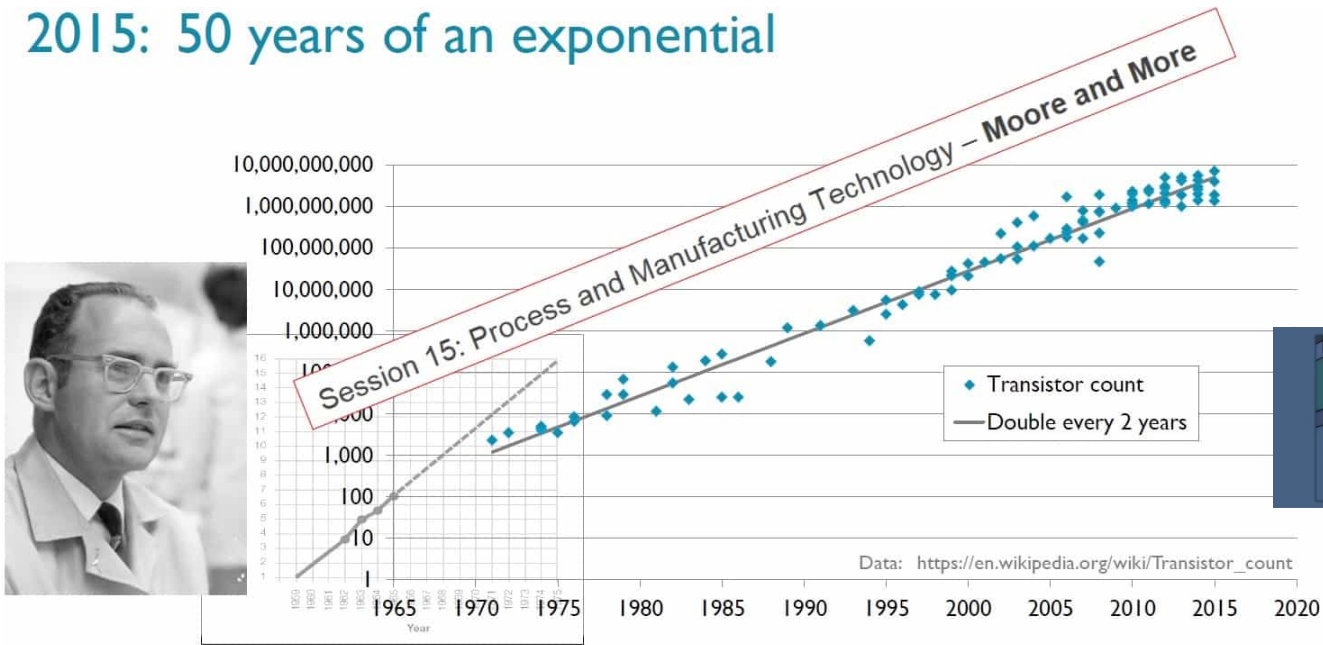


Performance increase by factor of 1865



Moore's Law

- Moore's Law: Number of transistors doubles every 18 months to 2 years
2015: 50 years of an exponential





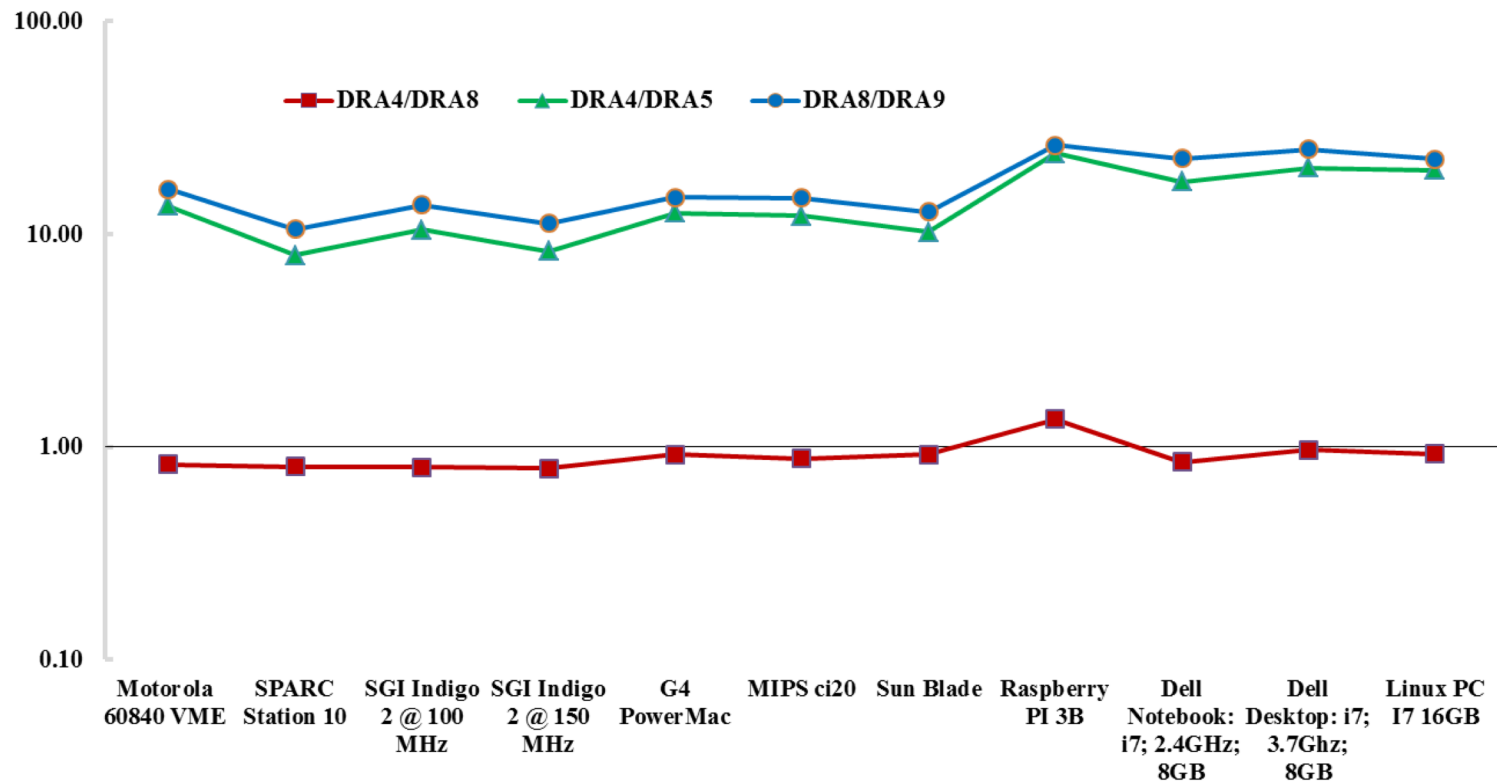
Moore's Law in Action

- Number of transistors doubles every 18 months to 2 years
- Computing power should similarly increase
- Observed decrease in processor time of 1865 since 1994 VME system
- **DRA 4 comparison**
 - VME Processor: 330 μ s
 - Sparc Station 10: 73 μ s
 - Raspberry Pi 3 Model B: 3.35 μ s
 - Modern Intel PC: 0.2 μ s
- **Decrease by factor of > 1600!**





Relative Performance of Dead Reckoning Algorithms

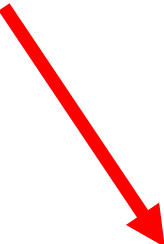




Ratios of DRA Times

- DRA 4 and DRA 5 similar performance
- DRA 9 much slower than DRA 5
- DRA 5 simple quadratic
- DRA 9 needs rotation matrices
- Floating Point Operations
 - DRA 4 99
 - DRA 5 43
 - DRA 8 177
 - DRA 9 115


$$P = P_0 + V_0 \Delta t + \frac{1}{2} A_0 \nabla t^2$$


$$P = P_0 + [R_0]_{w \rightarrow b}^{-1} ([R1]V_b + [R2]A_b)$$



Discussion

- Proposal for DIS version 8 to use single DRA for moving entities and geodetic coordinate system
- This would be similar to existing DRA 8 – the slowest algorithm
- Modern PC only takes 0.2 μ s (200 ns) for DRA 8
- Benchmark – use modern PC: 2017 Intel i7 7600U; dual core operating at 3.9 GHz; 16 GB RAM

Algorithm	1	2	9	4	5	6	7	8	9
CPU Time (ns)	3.2	7.7	183.9	185.2	9.8	75.1	189.8	200.7	78.4

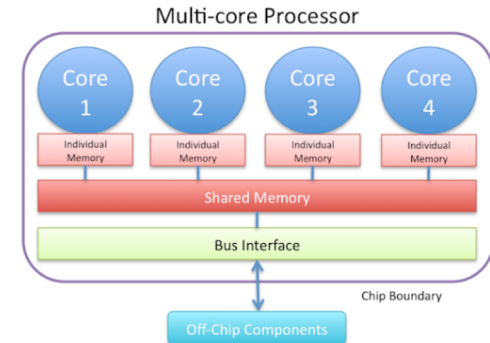


Multi-core Systems and Parallelism

- Have only considered single-threaded dead-reckoning performance
- Parallelism can also be used to increase speed of dead reckoning
- This involves running multiple instances of the dead reckoning algorithm across multiple threads or cores
- More sophisticated parallelism would require rewriting the dead reckoning implementation software to use vector-based instructions (eg Intel AVX-512)

Intel® Advanced Vector Extension (AVX)
256-bit vector extension to SSE for FP intensive applications

KEY FEATURES	BENEFITS
Wider Vectors Increased from 128 bit to 256 bit	Up to 2x peak FLOPs output
Enhanced Data Rearrangement Use the new 256 bit primitives to broadcast, mask, blend and do data permutations	Organize, access and pull only necessary data more quickly and efficiently
Three Operand, Non Destructive Syntax Designed for efficiency and future extensibility	Fewer register copies, better register use, more opportunities for parallel loads and compute operations, smaller code size





Summary and Conclusion

- **Dead reckoning performance studied for a range of systems 1994 - 2018**
- **Dead reckoning performance in a simple modern system such as a Raspberry Pi is far superior to the most advanced 1994 systems**
- **Relative performance of standard algorithms shows similar trends with algorithms that use orientation always running far slower**
- **Results can be used to benchmark dead reckoning algorithms proposed for next generation of DIS and other simulation protocols such as Real Time Platform Reference Object Model**



Simulation Interoperability Standards Organization

"Simulation Interoperability & Reuse through Standards"

QUESTIONS



BACKUP SLIDES



Towers and Hines Paper



94-57

B10

HIGHLY DYNAMIC VEHICLES
IN A
REAL/SIMULATED VIRTUAL ENVIRONMENT

HyDy

EQUATIONS OF MOTION OF THE
DIS 2.0.3 DEAD RECKONING
ALGORITHMS



7 FEBRUARY 1994

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HyDy

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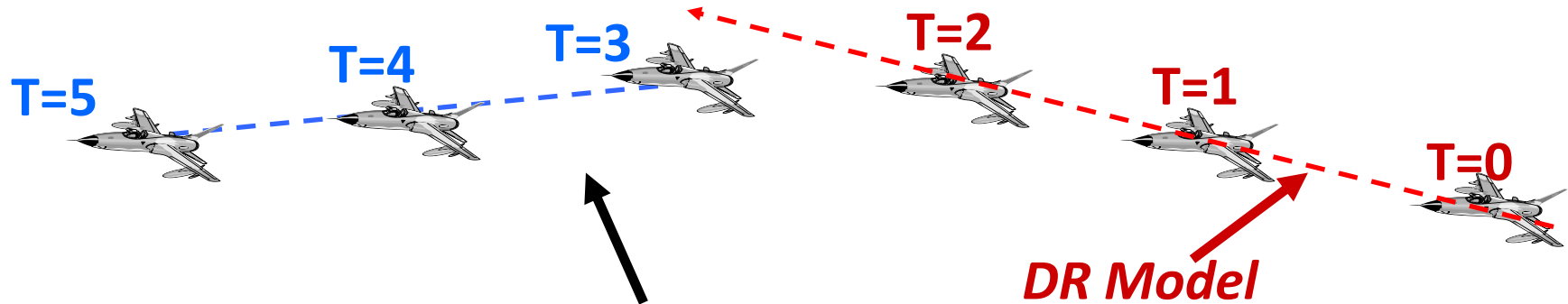


Part of Code Listing

```
/******\
*   File: performDR.c
*   Author: Jack Hines
*   Date: 06dec93 *
*   ETA Technologies
*   5505 Morehouse Dr. Suite 100
*   San Diego CA 92121
*   (619) 546-7800
*****
*   Description:
*       Dead reckons a single entity represented by a DIS 2.0.3 ESPDU.
*
*   Algorithm: Utilizes exact solution developed by Dr. John Towers
*               of Applied Data Technology Inc. and documented in
*               "Scientific and Technical Report for the Equations
*               of Motion of the DIS 2.0.3 Dead Reckoning Algorithms
*               of the HYDY Phase II Seamless Simulation (S2) Program",
*               SCITR-21-001, 17 July 1993. Equations involving body
*               coordinate velocity and acceleration have been changed
*               to eliminate effects of centripetal acceleration.
*               ( ie.  $V_b = \text{constant}$  when  $A_b = 0$ , and  $A_b = (d/dt)V_b$  )
*
*   Input Parameters: Pointer to the start of the ESPDU
*                   (EntityStatePDU *) (for entity DR)
*                   Time period for DR (seconds) *
*****/
```



Dead Reckoning in Action



***Entity State PDU broadcast;
Dead Reckoning Model updated***

DR Model



Results for Systems Tested

Algorithm execution times for all systems tested (ns)

Algorithm	PC: i7-5500; 2.4GHz; 8GB (Win10/ Cygwin)	PC: i7-3770; 3.7GHz; 8GB (Win7/ Cygwin)	RPI1 (Raspbian)	RPI2 (Raspbian)	RPI3A (Raspbian)	RP3B (Raspbian)	Ci20 (Debian)	PC: i7-7600; 16GB (Ubuntu)	Sun Blade (Debian)	G4 Power Mac (Ubuntu)
1	7.3	10.1	282.3	169.8	172.4	115.1	232.2	3.2	435.1	386.6
2	18.3	20.3	404.3	272.5	245.7	162.6	437.1	7.7	587.2	484.8
3	360.0	408.7	6270.8	4286.1	4520.9	3970.1	6360.1	184.0	6130.0	6589.1
4	380.7	366.0	6355.5	3732.3	4232.4	4519.2	6459.3	185.2	6190.4	6679.8
5	22.8	18.8	439.0	281.5	197.6	200.3	572.6	9.7	666.9	573.2
6	72.7	57.4	2791.9	1441.1	1415.7	1426.2	2661.9	75.1	2541.3	3085.7
7	422.0	335.6	6673.5	3926.2	3167.1	3260.6	6821.3	189.8	6330.9	6828.7
8	448.5	379.1	7097.4	4253.5	3320.9	3349.5	7360.8	200.7	6744.7	7278.6
9	89.4	81.5	2991.3	1542.4	1472.0	1485.1	2844.0	78.4	2674.5	3201.0



Proposed DRA 10 for DIS V8

- **Murray, R. E. (2018). Dead Reckoning in Geodetic Coordinates for Improved LVC Interoperability (18W-SIW-029). In: *2018 Winter Simulation Innovation Workshop*, Orlando, Florida, US: 21 - 26 Jan 2018**
- **DRA 10 proposed for DIS V8 as single algorithm for most moving entities**
- **Depends on DIS V8 using geodetic coordinates rather than geocentric**
- **Body-referenced**
- **Models acceleration in circular turns**
- **Straight and circular paths modeled better with DRA 10 and GDC system**



Moore's Law

- Moore, G. E. (1965) *Cramming more components onto integrated circuits. In Electronics 38 (8): 114–117.*
- Written in 1965
- Projects to 65000 components on single chip in 1975!

